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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,156	01/28/2004	Hirotaka Komatsubara	KAN 155	2155

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,156	KOMATSUBARA, HIROTAKA	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-13* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/28/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/04 and 4/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method for Manufacturing SOI LOCOS MOSFET with Metal Oxide Film or Impurity-Implanted Field Oxide.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Fig. 3C is missing a label for "a fluorine ion F 280," page 11, second full paragraph, line 3 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgener (U.S. 5,863,823) in view of Duffy (U.S. 3,809,574).

With respect to claim 5, Burgener teaches a method of manufacturing a semiconductor device using a LOCOS method for element isolation comprising the steps of: forming a pad oxide film (silicon dioxide layer 36 in Fig. 2A; column 6, line 28) and a nitride film (silicon nitride layer 32 in Fig. 2A; column 6, lines 28-29) sequentially on a silicon layer in an element region (silicon layer 28 in Fig. 2A; column 6, lines 29-30); forming a field oxide film in an element isolation region by implementing an oxidation treatment (silicon dioxide regions 34 in Fig. 2C; column 6, lines 45-48); and removing the nitride film and the pad oxide film (column 6, lines 52-54).

Burgener does not expressly teach forming a metal oxide film for generating a fixed electric charge on the nitride film and on the silicon layer in an element isolation region.

With respect to claim 5, Duffy teaches a process for forming a metal oxide film (column 1, line 61; column 5, line 3) for generating a fixed electric charge on the silicon

layer (column 5, lines 32-33; column 6, lines 50-51). The method is specifically taught to eliminate bias, a known problem in isolation (column 6, lines 50-51).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Burgener's method of manufacturing a semiconductor device by forming an aluminum oxide film for generating a fixed electric charge on the silicon layer in an element isolation region, as in claim 5 and as taught by Duffy. When applied to Burgener's method, the aluminum oxide film would inherently also generate a fixed electric charge on the nitride film. The motivation for doing so at the time of invention would have been to generate the fixed electric charge on the silicon layer to effect zero gate bias, as expressly taught by Duffy.

With respect to claim 6, Burgener teaches a method of manufacturing a semiconductor device on an ultrathin intrinsic silicon film provided on an insulating sapphire (aluminum oxide, Al_2O_3) substrate (column 3, lines 48-50) (the silicon layer is a silicon layer of an SOI structure formed on an insulating oxide layer). Together Burgener and Duffy teach claim 5, as addressed in the 35 U.S.C. 103(a) rejection above.

Therefore, it would have been obvious to combine Duffy with Burgener to develop a method of manufacturing a semiconductor device according to claim 5 wherein the silicon layer is a silicon layer of an SOI structure formed on an insulating oxide layer, as specified in claim 6, for the same reasons provided for claim 5 above.

With respect to claim 7, Burgener and Duffy together teach claim 5, as addressed in the 35 U.S.C. 103(a) rejection above. Burgener further teaches a method of manufacturing a semiconductor device wherein the element is an N-channel

MOSFET (column 6, lines 4-5, 26). Burgener does not expressly teach that the fixed electric charge is a negative electric charge.

With respect to claim 7, Duffy teaches that the fixed electric charge is a negative fixed electric charge (column 6, lines 50-51).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Burgener's method of manufacturing a semiconductor device by forming an aluminum oxide film for generating a negative fixed electric charge, as taught by Duffy, on the silicon layer in an N-channel MOSFET. The motivation for doing so at the time of invention would have been to generate the fixed electric charge on the silicon layer to effect zero gate bias (Duffy, column 5, lines 32-33; column 6, lines 50-51).

With respect to claim 8, Duffy teaches that the metal oxide film is aluminum oxide (column 1, line 61). Burgener and Duffy together teach claim 7, as addressed in the 35 U.S.C. 103(a) rejection above. Therefore, it would have been obvious at the time of invention to combine Duffy with Burgener to develop a method of manufacturing a semiconductor device according to claim 7 wherein the metal oxide film is aluminum oxide, as specified in claim 8, for the same reasons provided for claim 7 above.

Claims 9, 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgener (U.S. 5,863,823) in view of Nishioka (December 1990).

With respect to claim 9, Burgener teaches a method of manufacturing a semiconductor device using a LOCOS method for element isolation comprising the steps of: forming a pad oxide film (silicon dioxide layer 36 in Fig. 2A; column 6, line 28)

and a nitride film (silicon nitride layer 32 in Fig. 2A; column 6, lines 28-29) sequentially on a silicon layer in an element region (silicon layer 28 in Fig. 2A; column 6, lines 29-30); forming a field oxide film in an element isolation region by implementing an oxidation treatment (silicon dioxide regions 34 in Fig. 2C; column 6, lines 45-48); and removing the nitride film and the pad oxide film (column 6, lines 52-54).

Burgener does not expressly teach implanting an impurity into the field oxide film to generate a fixed electric charge on the field oxide film.

With respect to claim 9, Nishioka teaches a method of manufacturing a semiconductor device comprising the step of implanting an impurity into a field oxide film (page 2026, abstract) to generate a fixed electric charge in the field oxide film (page 2026, abstract). Nishioka teaches that the fluorination of the field oxide results in a smaller density of radiation-induced positive oxide charge compared to the control, which indicates that the fluorination contributes negative charges to the oxide. Nishioka teaches the advantage of using this method to increase the radiation hardness of the field oxide and thereby reduce the susceptibility of the field oxide to radiation-induced oxide charge and/or bias (page 2026, abstract).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Burgener's method of manufacturing a semiconductor device by implanting an impurity into the field oxide film, as in claim 9 and as taught by Nishioka. The motivation for doing so at the time of invention would have been to increase the radiation hardness of the field oxide, and reduce the susceptibility of the

field oxide to radiation-induced oxide charge and/or bias, as expressly taught by Nishioka.

With respect to claim 10, Burgener teaches a method of manufacturing a semiconductor device on an ultrathin intrinsic silicon film provided on an insulating sapphire (aluminum oxide, Al_2O_3) substrate (column 3, lines 48-50) (the silicon layer is a silicon layer of an SOI structure formed on an insulating oxide layer). Together Burgener and Nishioka teach claim 9, as addressed in the 35 U.S.C. 103(a) rejection above.

Therefore, it would have been obvious to combine Nishioka with Burgener to develop a method of manufacturing a semiconductor device according to claim 9 wherein the silicon layer is a silicon layer of an SOI structure formed on an insulating oxide layer, to obtain the invention as specified in claim 10, for the same reasons provided for claim 9 above.

With respect to claim 12, Burgener and Nishioka together teach claim 9, as addressed in the 35 U.S.C. 103(a) rejection above. Burgener further teaches a method of manufacturing a semiconductor device wherein the element is an N-channel MOSFET (column 6, lines 4-5, 26). Burgener does not expressly teach that the fixed electric charge is a negative fixed electric charge.

With respect to claim 12, Nishioka teaches a method of manufacturing a semiconductor device comprising the step of implanting an impurity into a field oxide wherein the fixed electric charge is a negative fixed electric charge. As stated above, Nishioka teaches that the fluorination of the field oxide results in a smaller density of radiation-induced positive oxide charge compared to the control, which indicates that

the fluorination contributes negative charges to the oxide, resulting in the advantage of increased radiation hardness (page 2026, abstract).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to apply modify Burgener's method of manufacturing a semiconductor device by implanting an impurity into the field oxide film to generate a negative fixed electric charge on the field oxide film, as in claim 12 and as taught by Nishioka, wherein the element is an N-channel MOSFET. The motivation for doing so at the time of invention would have been to increase the radiation hardness of the field oxide, or reduce the susceptibility of the field oxide to radiation-induced oxide charge and/or bias, as expressly taught by Nishioka.

With respect to claim 13, Burgener and Nishioka together teach claim 12, as addressed in the 35 U.S.C. 103(a) rejection above. Nishioka further teaches a method of manufacturing a semiconductor device comprising the step of implanting an impurity into a field oxide film wherein the impurity is a fluorine ion (page 2026, abstract). Therefore, it would have been obvious to combine Nishioka with Burgener to develop a method of manufacturing a semiconductor device according to claim 12 wherein the impurity is a fluorine ion, to obtain the invention as specified in claim 13, for the same reasons provided for claim 12 above.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burgener and Nishioka as applied to claims 9 and 10 above, and further in view of Chen (U.S. 5,899,723).

Together Burgener and Nishioka teach a method of manufacturing a semi-conductor device according to claim 9, as addressed in the 35 U.S.C. 103(a) rejection above.

Burgener and Nishioka do not teach a method of manufacturing a semiconductor device wherein the impurity is implanted by a diagonal ion implantation.

With respect to claim 11, Chen teaches a method of manufacturing a semiconductor device wherein an impurity is introduced by a diagonal ion implantation (Fig. 3b; column 3, lines 33-34).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the semiconductor process of claim 9, as taught by Burgener and Nishioka, by using diagonal ion implantation, as taught by Chen. The motivation for doing so at the time of invention would have been to implant impurities on a slanted surface, as shown in Chen's Fig. 3b.

Therefore, it would have been obvious to combine Chen with Nishioka and Burgener for the benefit of creating a method of manufacturing a semiconductor device according to claim 9 wherein the impurity is implanted by a diagonal ion implantation, to obtain the invention as specified in claim 11.

Cited Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

D. Niu, et al. (May 2002) teach interface reactions of Al_2O_3 on silicon, including a mechanism for silicon to diffuse through the Al_2O_3 layer and oxidize.

Blanchard, et al. (EP0213972) teach a method for shifting the threshold voltage of DMOS transistors by implanting ions into the gate oxide.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER